Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 4, 8, 9, 11, 13, 17, 21, 22, 24, 31, 34, 36, 37, 38, 40, 47, 50, 52, 53 and 57 as follows:

Listing of Claims:

1. (Currently Amended) A data receiver ~~coupled~~ to received data at a data bus port, the data receiver comprising:

a clock generator generating a receive clock signal, the clock generator including a phase adjust input to adjust the phase of the receive clock signal responsive to a phase adjust signal applied to the phase adjust input;

an expected pattern memory storing an expected data pattern;

a receive capture buffer coupled to the data bus port, the receive capture buffer being operable responsive to the receive clock signal to capture data coupled to the data bus port, including a plurality of sequentially received data patterns;

a pattern comparator coupled to the receive capture buffer and to the expected pattern memory, the pattern comparator being operable to compare the captured data patterns to the expected data pattern stored in the expected pattern memory and to generate a results signal indicative of the results of each of the comparisons;

phase adjustment logic coupled to the receive clock generator and to the pattern comparator to receive the results signal from the pattern comparator, the phase adjustment logic being operable to output the phase adjust signal; and

a receive interface controller coupled to the pattern comparator and to the phase adjustment logic, the receiver interface controller being operable in an initialization mode to cause the phase adjustment logic to sequentially output a plurality of phase adjust signals to cause the receive clock generator to incrementally alter the phase of the receive clock signal to allow the receive interface controller to determine based on the results signal from the pattern comparator the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern stored in the expected pattern memory, the receive interface

controller further being operable to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receive interface controller being operable in a normal operating mode to cause the phase adjustment logic to output a phase adjust signal that causes the receive clock generator to set the phase of the receive clock signal to the final phase value.

2. (Original) The receiver of claim 1 wherein the receive capture buffer comprises:

a plurality of flip-flops corresponding in number to the number of data bits of the data bus port, each of the flip-flops having a data input coupled to a respective bit of the data bus port, each of the flip-flops further having a clock input to which the receive clock is applied, the flip-flops being operable to capture the respective data bits responsive to transitions of the receive clock signal; and

a recirculating buffer coupled to receive and store a plurality of data bits sequentially captured by at least one of the flip-flops, the recirculating buffer being operable to couple the data bits stored in the recirculating buffer to the pattern comparator.

3. (Original) The receiver of claim 2 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal and is operable to generate the receive clock signal from the reference clock signal.

4. (Currently Amended) The receiver of claim 3, further comprising a multiplexer ~~coupled~~ to receive the stored data bits from the recirculating buffer, the multiplexer being operable to select one of a plurality of subsets of the stored data bits for transmitting~~coupling~~ to the pattern comparator.

5. (Original) The receiver of claim 4 wherein the number N of data bits in each of the subsets is given by the formula:

$$N=[(f_1*m)/(f_2)]$$

Where f_1 is the frequency of the receive clock signal, f_2 is the frequency of the reference clock signal, and m is the number of data bits captured by the flip-flops during each period of the receive clock signal.

6. (Original) The receiver of claim 1 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal, and wherein the clock generator is operable to generate the receive clock signal from the reference clock signal.

7. (Original) The receiver of claim 1 wherein the receive interface controller is operable to initially alter the phase of the receive clock signal so that it is unable to capture received data patterns that match the expected data pattern, to then incrementally change the phase of the receive clock signal until the phase of the receive clock signal has a first phase value that it is able to capture receive data patterns that match the expected data pattern, and to continue incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a second phase value that it is unable to capture received data patterns that match the expected data pattern.

8. (Currently Amended) The receiver of claim 7 wherein the receive interface controller is operable to select as the final value for the phase of the receive clock signal a phase value that is ~~substantially~~ intermediate the first and second phase values.

9. (Currently Amended) A memory module, comprising:

a receiver coupled to a downstream data bus port, the receiver being operable to capture data coupled to the downstream data bus port, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match a first

predetermined data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the first predetermined data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value;

a transmitter coupled to an upstream data bus port, the transmitter being operable in the initialization mode to generate a second predetermined data pattern and to repeatedly couple the generated data pattern to the upstream data bus port;

a plurality of memory devices; and

a memory hub coupled to the transmitter and the receiver, the memory hub comprising:

a bus interface coupled to the receiver and the transmitter, the bus interface being operable to receive write data from the receiver and to couple read data to the transmitter; and

a memory device interface coupled to the bus interface and the memory devices, the memory device interface transmitting~~coupling~~ the write data to the memory devices and coupling the read data from the memory devices.

10. (Original) The memory module of claim 9 wherein the receiver comprises:

a clock generator generating a receive clock signal, the clock generator including a phase adjust input to adjust the phase of the receive clock signal responsive to a phase adjust signal applied to the phase adjust input;

an expected pattern memory storing the first predetermined data pattern;

a receive capture buffer coupled to the downstream data bus port, the receive capture buffer being operable to capture data coupled to the downstream data bus port, including a plurality of sequentially received data patterns;

a pattern comparator coupled to the receive capture buffer and to the expected pattern memory, the pattern comparator being operable to compare the captured data patterns to

the first predetermined data pattern stored in the expected pattern memory and to generate a results signal indicative of the results of each of the comparisons;

phase adjustment logic coupled to the receive clock generator and to the pattern comparator to receive the results signal from the pattern comparator, the phase adjustment logic being operable to output the phase adjust signal; and

a receive interface controller coupled to the pattern comparator and to the phase adjustment logic, the receive interface controller being operable in an initialization mode to cause the phase adjustment logic to sequentially output a plurality of phase adjust signals to cause the receive clock generator to incrementally alter the phase of the receive clock signal to allow the receive interface controller to determine based on the results signal from the pattern comparator the phases of the receive clock signal that are able to capture received data patterns that match the first predetermined data pattern stored in the expected pattern memory, the receive interface controller further being operable to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the first predetermined data pattern, the receive interface controller being operable in a normal operating mode to cause the phase adjustment logic to output a phase adjust signal that causes the receive clock generator to set the phase of the receive clock signal to the final phase value.

11. (Currently Amended) The memory module of claim 10 wherein the receive capture buffer comprises:

a plurality of flip-flops corresponding in number to the number of data bits of the downstream data bus port, each of the flip-flops having a data input coupled to a respective bit of the downstream data bus port, each of the flip-flops further having a clock input to which the receive clock is applied, the flip-flops being operable to capture the respective data bits responsive to transitions of the receive clock signal; and

a recirculating buffer ~~coupled~~ to receive and store a plurality of data bits sequentially captured by at least one of the flip-flops, the recirculating buffer being operable to couple the data bits stored in the recirculating buffer to the pattern comparator.

12. (Original) The memory module of claim 11 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal and is operable to generate the receive clock signal from the reference clock signal.

13. (Currently Amended) The memory module of claim 12, further comprising a multiplexer coupled to receive the stored data bits from the recirculating buffer, the multiplexer being operable to select one of a plurality of subsets of the stored data bits for transmitting~~coupling~~ to the pattern comparator.

14. (Original) The memory module of claim 13 wherein the number N of data bits in each of the subsets is given by the formula:

$$N=[(f_1*m)/(f_2)]$$

Where f_1 is the frequency of the receive clock signal, f_2 is the frequency of the reference clock signal, and m is the number of data bits captured by the flip-flops during each period of the receive clock signal.

15. (Original) The memory module of claim 10 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal, and wherein the clock generator is operable to generate the receive clock signal from the reference clock signal.

16. (Original) The memory module of claim 10 wherein the receive interface controller is operable to initially alter the phase of the receive clock signal so that it is unable to capture received data patterns that match the first predetermined data pattern, to then incrementally change the phase of the receive clock signal until the phase of the receive clock signal has a first phase value that it is able to capture received data patterns that match the first predetermined data pattern, and to continue incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a second phase value that it is unable to capture received data patterns that match the first predetermined data pattern.

17. (Currently Amended) The memory module of claim 16 wherein the receive interface controller is operable to select as the final value for the phase of the receive clock signal a phase value that is ~~substantially~~ intermediate the first and second phase values.

18. (Original) The memory module of claim 9 wherein the transmitter comprises:

a pattern generator operable to generate second predetermined patterns of data; and

a transmit interface controller coupled to the pattern generator, the transmit interface controller being operable to cause the transmit interface controller to repeatedly generate the second predetermined data pattern and couple the generated data patterns to the upstream bus port.

19. (Original) The memory module of claim 9 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

20. (Original) The memory module of claim 9 wherein the first and second data patterns are identical to each other.

21. (Currently Amended) A memory system, comprising:

a first upstream data bus;

a first downstream data bus;

a memory hub controller, comprising:

a receiver coupled to the first upstream data bus, the receiver being operable to capture data ~~coupled~~ applied to the first upstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match a first data pattern, the receiver further being

operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the first data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value;

a transmitter coupled to the first downstream data bus, the transmitter being operable in the initialization mode to generate a second data pattern and to repeatedly couple the generated data pattern to the first downstream data bus;

a memory module comprising:

a receiver coupled to the first downstream data bus, the receiver being operable to capture data ~~coupled~~ applied to the first downstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the second data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the second data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value;

a transmitter coupled to the first upstream data bus, the transmitter being operable in the initialization mode to generate the first data pattern and to repeatedly couple the generated data pattern to the first upstream data bus;

a plurality of memory devices; and

a memory hub coupled to the transmitter in the memory module and the receiver in the memory module, the memory hub comprising:

a bus interface coupled to the receiver in the memory module and the transmitter in the memory module, the bus interface being operable to receive write data from the receiver in the memory module and to couple read data to the transmitter in the memory module; and

a memory device interface coupled to the bus interface and the memory devices, the memory device interface transmitting~~coupling~~ the write data to the memory devices and receiving~~coupling~~ the read data from the memory devices.

22. (Currently Amended) The memory system of claim 21 wherein the receiver in the memory controller is identical to the receiver ~~in the receiver~~ in the memory module, and wherein the transmitter in the memory controller is identical to the transmitter ~~in the receiver~~ in the memory module.

23. (Original) The memory system of claim 22 wherein the first and second data patterns are identical to each other and comprises an expected data pattern.

24. (Currently Amended) The memory system of claim 21 ~~23~~ wherein the receivers comprise:

a clock generator generating a receive clock signal, the clock generator including a phase adjust input to adjust the phase of the receive clock signal responsive to a phase adjust signal applied to the phase adjust input;

an expected pattern memory storing the expected data pattern;

a receive capture buffer coupled to the data bus to which the receiver is coupled, the receive capture buffer being operable to capture data ~~coupled~~ applied to the data bus, including a plurality of sequentially received data patterns;

a pattern comparator coupled to the receive capture buffer and to the expected pattern memory, the pattern comparator being operable to compare the captured data patterns to the expected data pattern stored in the expected pattern memory and to generate a results signal indicative of the results of each of the comparisons;

phase adjustment logic coupled to the receive clock generator and to the pattern comparator to receive the results signal from the pattern comparator, the phase adjustment logic being operable to output the phase adjust signal; and

a receive interface controller coupled to the pattern comparator and to the phase adjustment logic, the receive interface controller being operable in an initialization mode to cause the phase adjustment logic to sequentially output a plurality of phase adjust signals to cause the receive clock generator to incrementally alter the phase of the receive clock signal to allow the receive interface controller to determine based on the results signal from the pattern comparator the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern stored in the expected pattern memory, the receive interface controller further being operable to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receive interface controller being operable in a normal operating mode to cause the phase adjustment logic to output a phase adjust signal that causes the receive clock generator to set the phase of the receive clock signal to the final phase value.

25. (Original) The memory system of claim 24 wherein the receive capture buffer comprises:

a plurality of flip-flops corresponding in number to the number of data bits of the respective data bus, each of the flip-flops having a data input coupled to a respective bit of the respective data bus, each of the flip-flops further having a clock input to which the receive clock is applied, the flip-flops being operable to capture the respective data bits responsive to transitions of the receive clock signal; and

a recirculating buffer coupled to receive and store a plurality of data bits sequentially captured by at least one of the flip-flops, the recirculating buffer being operable to couple the data bits stored in the recirculating buffer to the pattern comparator.

26. (Original) The memory system of claim 25 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal and is operable to generate the receive clock signal from the reference clock signal.

27. (Original) The memory system of claim 26, further comprising a multiplexer coupled to receive the stored data bits from the recirculating buffer, the multiplexer being operable to select one of a plurality of subsets of the stored data bits for coupling to the pattern comparator.

28. (Original) The memory system of claim 27 wherein the number N of data bits in each of the subsets is given by the formula:

$$N=[(f_1*m)/(f_2)]$$

Where f_1 is the frequency of the receive clock signal, f_2 is the frequency of the reference clock signal, and m is the number of data bits captured by the flip-flops during each period of the receive clock signal.

29. (Original) The memory system of claim 24 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal, and wherein the clock generator is operable to generate the receive clock signal from the reference clock signal.

30. (Original) The memory system of claim 24 wherein the receive interface controller is operable to initially alter the phase of the receive clock signal so that it is unable to capture received data patterns that match the expected data pattern, to then incrementally change the phase of the receive clock signal until the phase of the receive clock signal has a first phase value that it is able to capture received data patterns that match the expected data pattern, and to continue incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a second phase value that it is unable to capture received data patterns that match the expected data pattern.

31. (Currently Amended) The memory system of claim 30 wherein the receive interface controller is operable to select as the final value for the phase of the receive clock signal a phase value that is ~~substantially~~ intermediate the first and second phase values.

32. (Original) The memory system of claim 23 wherein the transmitter comprises:

a pattern generator operable to generate the expected data pattern; and

a transmit interface controller coupled to the pattern generator, the transmit interface controller being operable to cause the transmit interface controller to repeatedly generate the expected data pattern and couple the generated data patterns to the data bus to which the transmitter is coupled.

33. (Original) The memory system of claim 21 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

34. (Currently Amended) The memory system of claim 21~~23~~, further comprising:

a second upstream data bus;

a second downstream data bus; and

wherein the first memory module further comprises:

a second receiver coupled to a second upstream data bus, the second receiver being operable to capture data coupled to the second upstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value; and

a second transmitter coupled to the second downstream data bus, the second transmitter being operable in the initialization mode to generate the expected data

pattern and to repeatedly couple the generated data pattern to the second downstream data bus.

35. (Original) The memory system of claim 34 wherein the memory module further comprises:

a downstream bypass path coupling the first downstream data bus to the second downstream data bus; and

an upstream bypass path coupling the first upstream data bus to the second upstream data bus.

36. (Currently Amended) The memory system of claim 34, further comprising a second memory module coupled to the second downstream data bus and the second upstream data bus, the second memory module comprising:

a receiver coupled to the second downstream data bus, the receiver being operable to capture data ~~coupled~~ applied to the second downstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value; and

a transmitter coupled to the second upstream data bus, the transmitter being operable in the initialization mode to generate the expected data pattern and to repeatedly couple the generated data pattern to the second upstream data bus.

a plurality of memory devices; and

a memory hub coupled to the transmitter and the receiver, the memory hub comprising:

a bus interface coupled to the receiver and the transmitter, the bus interface being operable to receive write data from the receiver and to couple read data to the transmitter; and

a memory device interface coupled to the bus interface and the memory devices, the memory device interface transmitting~~coupling~~ the write data to the memory devices and receiving~~coupling~~ the read data from the memory devices.

37. (Currently Amended) A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a first upstream data bus;

a first downstream data bus;

a memory hub controller coupled to the processor bus, the memory hub controller comprising:

a receiver coupled to the first upstream data bus, the receiver being operable to capture data ~~coupled~~ applied to the first upstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match a first data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive

clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the first data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value;

a transmitter coupled to the first downstream data bus, the transmitter being operable in the initialization mode to generate a second data pattern and to repeatedly couple the generated data pattern to the first downstream data bus; and

a memory module, comprising:

a receiver coupled to the first downstream data bus, the receiver being operable to capture data ~~coupled~~ applied to the first downstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the second data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the second data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value;

a transmitter coupled to the first upstream data bus, the transmitter being operable in the initialization mode to generate the first data pattern and to repeatedly couple the generated data pattern to the first upstream data bus;

a plurality of memory devices; and

a memory hub coupled to the transmitter in the memory module and the receiver in the memory module, the memory hub comprising:

a bus interface coupled to the receiver in the memory module and the transmitter in the memory module, the bus interface being operable to receive write data from the receiver and to couple read data to the transmitter; and

a memory device interface coupled to the bus interface and the memory devices, the memory device interface transmitting~~coupling~~ the write data

to the memory devices and receiving ~~coupling~~ the read data from the memory devices.

38. (Currently Amended) The memory system of claim 37 wherein the receiver in the memory controller is identical to the receiver ~~in the receiver~~ in the memory module, and wherein the transmitter in the memory controller is identical to the transmitter ~~in the receiver~~ in the memory module.

39. (Original) The memory system of claim 38 wherein the first and second data patterns are identical to each other and comprises an expected data pattern.

40. (Currently Amended) The memory system of claim 37~~23~~ wherein the receivers comprise:

a clock generator generating a receive clock signal, the clock generator including a phase adjust input to adjust the phase of the receive clock signal responsive to a phase adjust signal applied to the phase adjust input;

an expected pattern memory storing the expected data pattern;

a receive capture buffer coupled to the data bus to which the receiver is coupled, the receive capture buffer being operable to capture data ~~coupled~~ applied to the data bus, including a plurality of sequentially received data patterns;

a pattern comparator coupled to the receive capture buffer and to the expected pattern memory, the pattern comparator being operable to compare the captured data patterns to the expected data pattern stored in the expected pattern memory and to generate a results signal indicative of the results of each of the comparisons;

phase adjustment logic coupled to the receive clock generator and to the pattern comparator to receive the results signal from the pattern comparator, the phase adjustment logic being operable to output the phase adjust signal; and

a receive interface controller coupled to the pattern comparator and to the phase adjustment logic, the receive interface controller being operable in an initialization mode to

cause the phase adjustment logic to sequentially output a plurality of phase adjust signals to cause the receive clock generator to incrementally alter the phase of the receive clock signal to allow the receive interface controller to determine based on the results signal from the pattern comparator the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern stored in the expected pattern memory, the receive interface controller further being operable to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receive interface controller being operable in a normal operating mode to cause the phase adjustment logic to output a phase adjust signal that causes the receive clock generator to set the phase of the receive clock signal to the final phase value.

41. (Original) The memory system of claim 40 wherein the receive capture buffer comprises:

a plurality of flip-flops corresponding in number to the number of data bits of the respective data bus, each of the flip-flops having a data input coupled to a respective bit of the respective data bus, each of the flip-flops further having a clock input to which the receive clock is applied, the flip-flops being operable to capture the respective data bits responsive to transitions of the receive clock signal; and

a recirculating buffer coupled to receive and store a plurality of data bits sequentially captured by at least one of the flip-flops, the recirculating buffer being operable to couple the data bits stored in the recirculating buffer to the pattern comparator.

42. (Original) The memory system of claim 41 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal and is operable to generate the receive clock signal from the reference clock signal.

43. (Original) The memory system of claim 42, further comprising a multiplexer coupled to receive the stored data bits from the recirculating buffer, the multiplexer

being operable to select one of a plurality of subsets of the stored data bits for coupling to the pattern comparator.

44. (Original) The memory system of claim 43 wherein the number N of data bits in each of the subsets is given by the formula:

$$N=[(f_1*m)/(f_2)]$$

Where f_1 is the frequency of the receive clock signal, f_2 is the frequency of the reference clock signal, and m is the number of data bits captured by the flip-flops during each period of the receive clock signal.

45. (Original) The memory system of claim 40 wherein the clock generator receives a reference clock signal having a lower frequency than the receive clock signal, and wherein the reference generator is operable to generate the receive clock signal from the reference clock signal.

46. (Original) The memory system of claim 40 wherein the receive interface controller is operable to initially alter the phase of the receive clock signal so that it is unable to capture received data patterns that match the expected data pattern, to then incrementally change the phase of the receive clock signal until the phase of the receive clock signal has a first phase value that it is able to capture received data patterns that match the expected data pattern, and to continue incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a second phase value that it is unable to capture received data patterns that match the expected data pattern.

47. (Currently Amended) The memory system of claim 46 wherein the receive interface controller is operable to select as the final value for the phase of the receive clock signal a phase value that is ~~substantially~~ intermediate the first and second phase values.

48. (Original) The memory system of claim 39 wherein the transmitter comprises:

a pattern generator operable to generate the expected data pattern; and

a transmit interface controller coupled to the pattern generator, the transmit interface controller being operable to cause the transmit interface controller to repeatedly generate the expected data pattern and couple the generated data patterns to the data bus to which the transmitter is coupled.

49. (Original) The memory system of claim 37 wherein the plurality of memory devices comprises a plurality of synchronous random access memory devices.

50. (Currently Amended) The memory system of claim 39, further comprising:

a second upstream data bus;

a second downstream data bus; and

wherein the first memory module further comprises:

a second receiver coupled to a second upstream data bus, the second receiver being operable to capture data ~~coupled~~ applied to the second upstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value; and

a second transmitter coupled to the second downstream data bus, the second transmitter being operable in the initialization mode to generate the expected data

pattern and to repeatedly couple the generated data pattern to the second downstream data bus.

51. (Original) The memory system of claim 50 wherein the memory module further comprises:

a downstream bypass path coupling the first downstream data bus to the second downstream data bus; and

an upstream bypass path coupling the first upstream data bus to the second upstream data bus.

52. (Currently Amended) The memory system of claim 50, further comprising a second memory module coupled to the second downstream data bus and the second upstream data bus, the second memory module comprising:

a receiver coupled to the second downstream data bus, the receiver being operable to capture data coupled to the second downstream data bus, including a plurality of sequentially received data patterns, responsive to a receive clock signal, the receiver being operable in an initialization mode to incrementally alter the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable in the initialization mode to determine a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern, the receiver further being operable to set the phase of the receive clock signal to the final phase value; and

a transmitter coupled to the second upstream data bus, the transmitter being operable in the initialization mode to generate the expected data pattern and to repeatedly couple the generated data pattern to the second upstream data bus.

a plurality of memory devices; and

a memory hub coupled to the transmitter and the receiver, the memory hub comprising:

a bus interface coupled to the receiver and the transmitter, the bus interface being operable to receive write data from the receiver and to couple read data to the transmitter; and

a memory device interface coupled to the bus interface and the memory devices, the memory device interface transmitting~~coupling~~ the write data to the memory devices and receiving~~coupling~~ the read data from the memory devices.

53. (Currently Amended) A method of capturing data in a memory system component, comprising:

coupling data to the memory system component, including repeatedly coupling an expected data pattern to the memory system component;

attempting to capture~~capturing~~ the data ~~coupled~~ applied to the memory system component ~~module~~ responsive to transitions of a receive clock signal;

incrementally altering the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern;

determining a final value for the phase of the receive clock signal based on the determination of the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern; and

using the final value of the phase of the receive clock signal to capture data ~~coupled~~applied to the memory system component.

54. (Original) The method of claim 53 wherein the memory system component comprises a memory hub controller.

55. (Original) The method of claim 53 wherein the memory system component comprises a memory module.

56. (Original) The method of claim 53 wherein the act of incrementally altering the phase of the receive clock signal to determine the phases of the receive clock signal that are able to capture received data patterns that match the expected data pattern comprises:

initially altering the phase of the receive clock signal so that it is unable to capture received data patterns that match the expected data pattern;

incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a first phase value that it is able to capture received data patterns that match the expected data pattern; and

continue incrementally changing the phase of the receive clock signal until the phase of the receive clock signal has a second phase value that it is unable to capture received data patterns that match the expected data pattern.

57. (Currently Amended) The method of claim 56 wherein the act of determining a final value for the phase of the receive clock signal comprises determining the final value for the phase of the receive clock signal as a phase value that is ~~substantially~~ intermediate the first and second phase values.